CLAIMS

What is claimed is:

1. A data access system for accessing data stored in a first and a second memory devices wherein:

said first and second memory devices having a difference of latency ΔL constituting a time-duration by which said first memory device starts an initial data access earlier than in said second memory device; and

a data access means for simultaneously accessing data in said first and second memory devices and for stopping accessing data in said first memory device once a data access operation has begun in said second memory device whereby said first memory device storing data only accessed initially in a time duration corresponding substantially to said difference of latency ΔL.

2. The data access system of claim 1 wherein:

said first and second memory devices having substantially a same continuous data access rate after said initial data accesses in said first and second memory devices are completed.

3. The data access system of claim 1 wherein:

said second memory device comprising a dynamic random access memory (DRAM) and said first memory device comprising a static random access memory (SRAM).

4. The data access system of claim 3 wherein:

said DRAM comprising a plurality of rows and said SRAM storing first several data of a plurality of rows in said DRAM and said DRAM storing data of a plurality of entire rows in said DRAM.

5. A data memory system comprising:

a dynamic random access memory (DRAM) and a static random access memory (SRAM) wherein said DRAM comprising a plurality of rows and said SRAM storing first several data of a plurality of rows in said DRAM and said DRAM storing data of a plurality of entire rows in said DRAM.

6. The data memory system of claim 5 further comprising:

a data access means simultaneously accessing data in said DRAM and said SRAM for stopping a data access from said SRAM when an initial data access in said DRAM begins.

7. The data memory system of claim 5 further comprising:

a data access means for checking data access instructions for sending said data access instructions directly to said DRAM when a data access is for a data stored in a same row compared to a previous data access instruction.

8. The data memory system of claim 5 further comprising:

a data access means for checking data access instructions for sending said data access instructions to said SRAM and DRAM when a data access is for a data stored in a different row compared to a previous data access instruction.

9. The data memory system of claim 5 wherein:

said SRAM storing first several data of a plurality of rows in said DRAM for accessing data from said SRAM during a DRAM latency period; and

said DRAM storing data of a plurality of entire rows in said DRAM for accessing data from said DRAM immediately after said DRAM latency period.

10. A method for accessing data stored in a first and a second memory devices having a difference of latency ΔL constituting a time-duration by which said first memory device starts an initial data access earlier than in said second memory device, comprising:

simultaneously accessing data in said first and second memory devices and stopping accessing data in second first memory device once an initial data access in said second memory device begins.

11. The method of claim 10 further comprising:

configuring said first and second memory devices having substantially a same continuous data access rate after said initial data accesses in said first and second memory devices are completed

12. The method of claim 10 wherein:

said step of accessing data from said second memory device is a step of accessing data from a dynamic random access memory (DRAM) and said step of access data from said first memory is a step of accessing data from a static random access memory (SRAM).

13. The method of claim 12 wherein:

said step of access data from said DRAM comprising a step of dividing said DRAM into a plurality of rows and storing a plurality of entire rows of data in said DRAM and storing in said SRAM first several data of a plurality of rows as that stored into said DRAM.

14. A method of configuring data memory system comprising:

dividing a dynamic random access memory (DRAM) into a plurality of rows for storing data into a plurality of entire rows and storing first several data from a plurality of said rows of said DRAM in a static random access memory (SRAM).

15. The method of claim 14 further comprising:

simultaneously sending data access instructions to said DRAM and said SRAM for simultaneously accessing data in said SRAM and DRAM and stopping accessing data in said SRAM once an initial data access begins in said DRAM.

16. The method of claim 14 further comprising:

checking data access instructions for sending said data access instructions directly to said DRAM when a data access is for a data stored in a same row compared to a previous data access instruction.

17. The method of claim 14 further comprising:

checking data access instructions for sending said data access instructions to said SRAM and DRAM when a data access is for a data stored in a different row compared to a previous data access instruction and stopping accessing data in said SRAM once an initial data access begins in said DRAM.

18. The method of claim 14 wherein:

said step of storing in said SRAM first several data of a plurality of rows in said DRAM is a step of accessing data stored in said SRAM during a DRAM latency period; and

storing in said DRAM a plurality of entire rows in said DRAM for accessing data from said DRAM immediately after said DRAM latency period.